User’s Guide

OPTIREG SBC TLE9271..4QX (V33)

About this document

Scope and purpose

The intention of this User's Guide is to provide relevant design-in information for automotive applications with the Infineon DCDC SBC family.

This User’s Guide covers the following products:

Table 1 Products

Sales name	SP Number	OPN
TLE9271QX	SP005729424	TLE9271QXXUMA2
TLE9271QX V33	SP005729488	TLE9271QXV33XUMA2
TLE9272QX	SP005729426	TLE9272QXXUMA2
TLE9272QX V33	SP005729516	TLE9272QXV33XUMA2
TLE9273QX	SP005729428	TLE9273QXXUMA2
TLE9273QX V33	SP005729528	TLE9273QXV33XUMA2
TLE9274QX	SP005729430	TLE9274QXXUMA3
TLE9274QX V33	SP005729539	TLE9274QXV33XUMA2

Intended audience

This document is for hardware engineers integrating devices of the DCDC SBC family into their applications.

Table of contents

1 Boost switch MOSFET selection for DCDC SBC

With datasheet revision 2.0 of DCDC SBC a short circuit detection on the BSTG pin is specified. Additionally a more detailed description of the gate driver strength is provided.

This chapter gives a guidance on how to select the correct MOSFET.

1.1 Use the recommended MOSFET

The gate driver parameters are optimized for the MOSFET BSS606N.
It is recommended to use this MOSFET.

1.2 Evaluate other MOSFET

In case there are reasons not to use the recommended MOSFET, the selection of other MOSFETs is limited by the short circuit protection at the gate driver as follows.

- The gate voltage needs to rise above a certain voltage within a certain time during charging.
- The gate voltage needs to fall below a certain voltage within a certain time during discharging.

The gate charge characteristic of the MOSFET and the gate driver strength both play a significant role in meeting the SBC gate short circuit timing requirements.

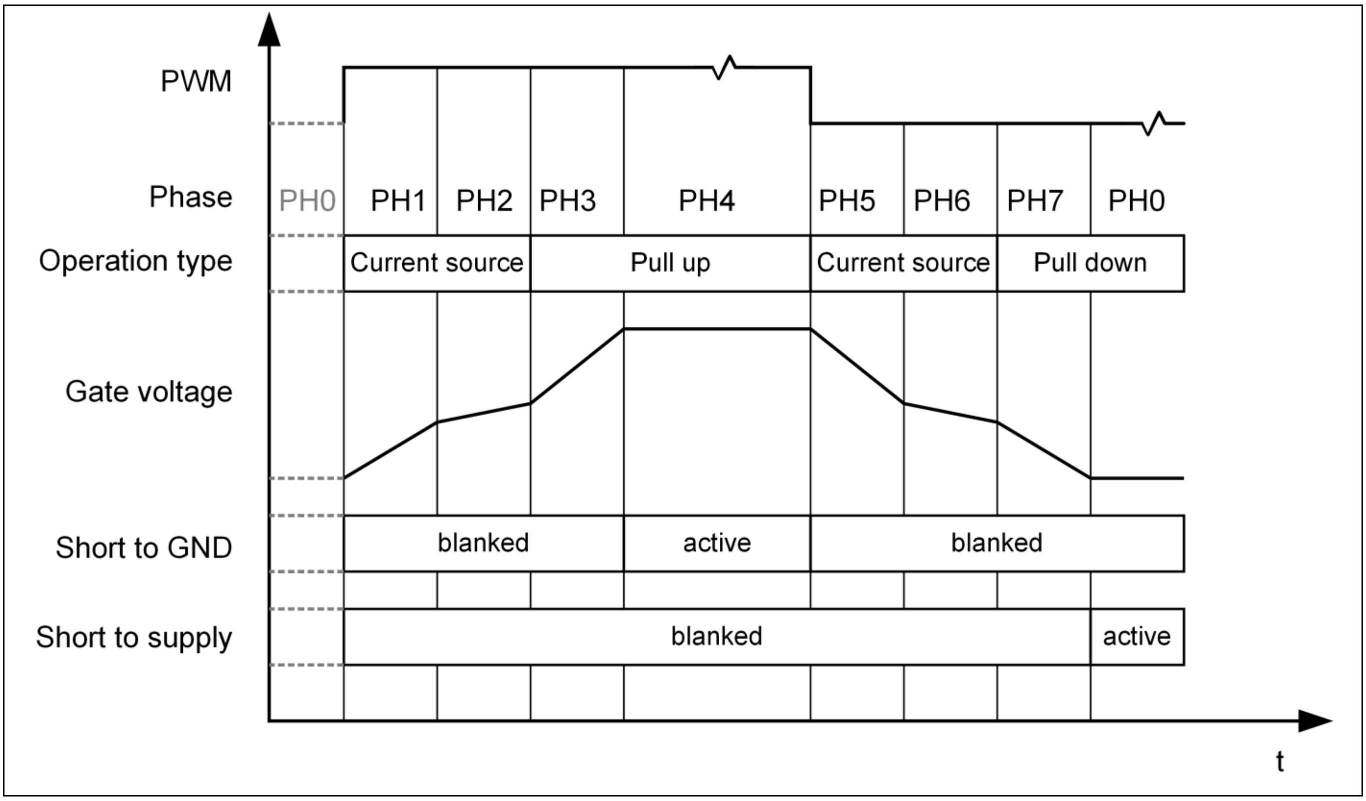

Figure 1 Phases of the boost switch gate driver

Because no minimum value for the driven current in the phases PH1, PH2, PH5, PH6 are given in the datasheet, it is recommended to execute the evaluation only with phases PH3 for charging and PH7 for discharging by SPICE simulation. The other phases should be considered as additional margin.

A proper simulation model of the MOSFET should be used, covering all needed operating conditions like temperature and production spread.

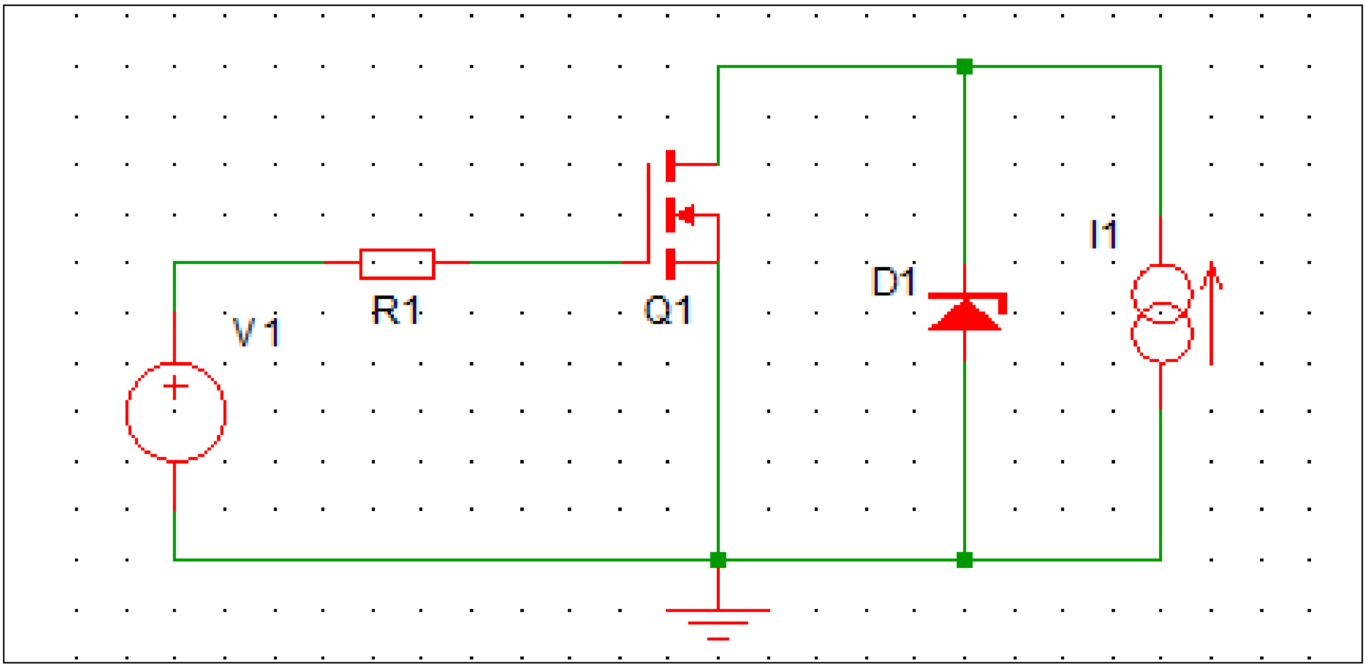

Figure 2 Simulation schematic

In Figure 2 a possible schematic for the evaluation is shown.

Q1 is the MOSFET under evaluation.

V1 in combination with R1 represents the pull up circuitry that is active in PH3 charging phase or the pull down circuitry of PH7 discharging phase respectively.
In the PH3 charging phase, V1 and R1 are datasheet parameters V_{drv_sup} and R_{PH3}.
In the PH7 discharging phase, V1 is ground and R1 is the datasheet parameter R_{PH7}.

I1 and D1 are used to set the operating point of the external MOSFET of the boost circuitry. I1 represents the coil current of the boost circuitry which has to be switched by Q1.

D1 limits the Q1 drain voltage to the boost output voltage (6.65V/8V/10V) when Q1 is OFF.

Following parameters may have impact on the evaluation result and therefore should be varied within the applicable range of the application:

- Temperature
- Drain voltage (Boost output voltage)
- Coil current
- Production spread of the external MOSFET

Figure 3 shows a possible simulation result for the charging curve.

Because the voltage on the gate (red curve) exceeds max{$V_{BSTG,sc}$} within min{t_{PH3}}, this operating point is evaluated with “pass”.

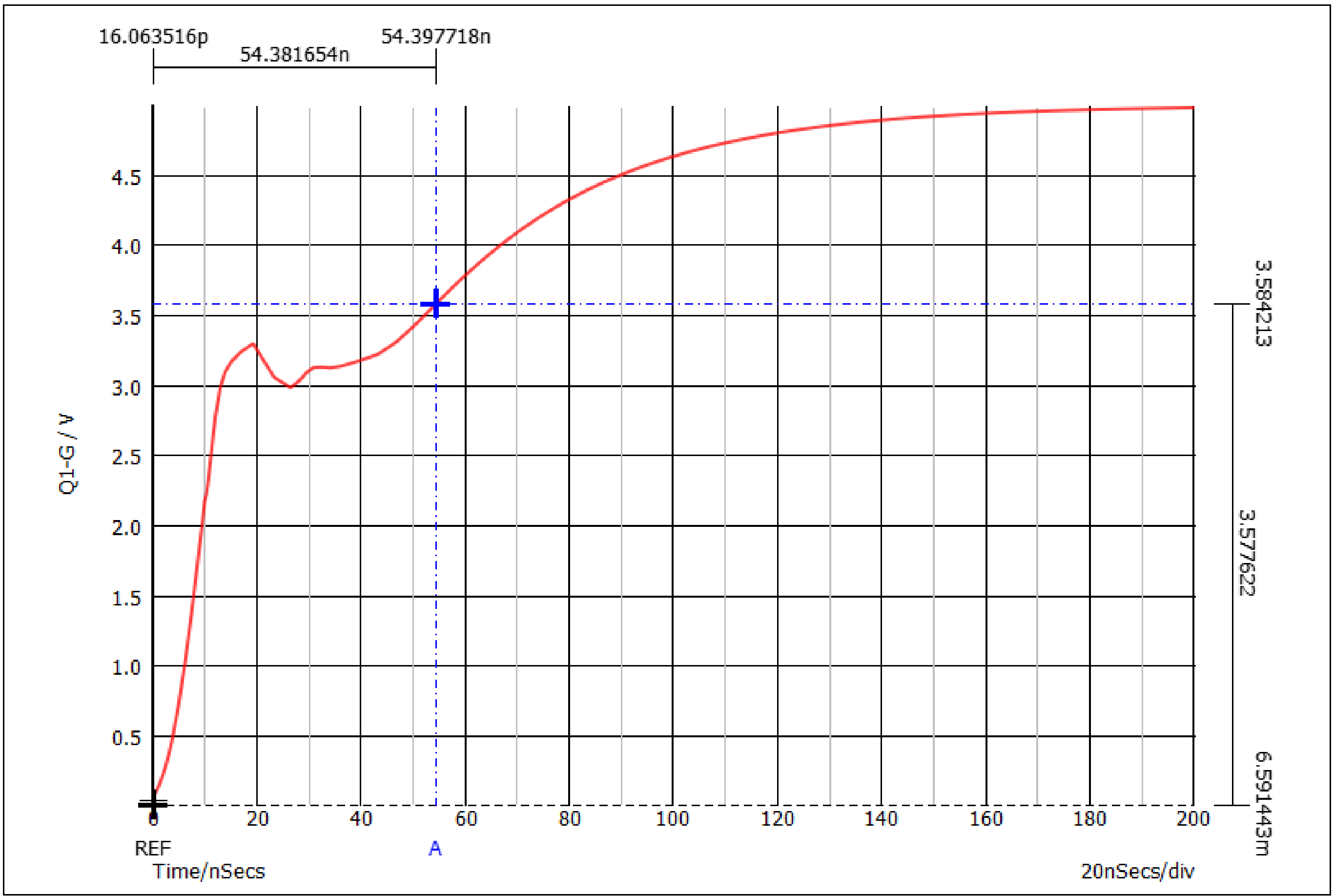

Figure 3 **Simulation result for charging (red=V_{BSTG})**

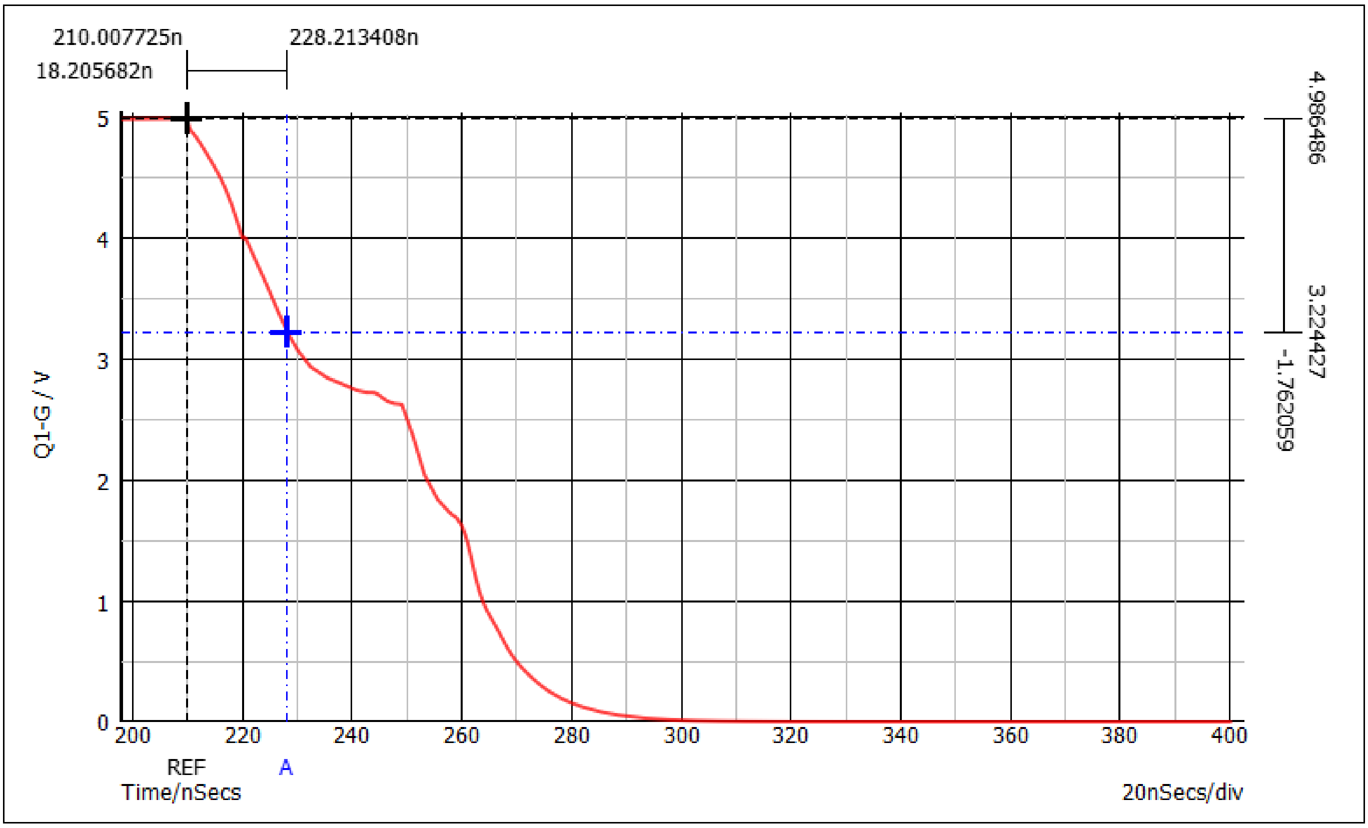

Figure 4 **Simulation result for discharging (red=V_{BSTG})**

Figure 4 shows a possible simulation result for discharging curve.

Because the voltage on the gate (red curve) is discharged below min{$V_{BSTG,sc}$} within min{t_{PH7}}, this operating point is evaluated with "pass".

1.3 Real measurement

A real measurement of the gate voltage measured at a board with BSS606N mounted can be seen in Figure 5. The markers measure the time from the start of the slope until the Miller plateau. It matches to the phase 1 timing.

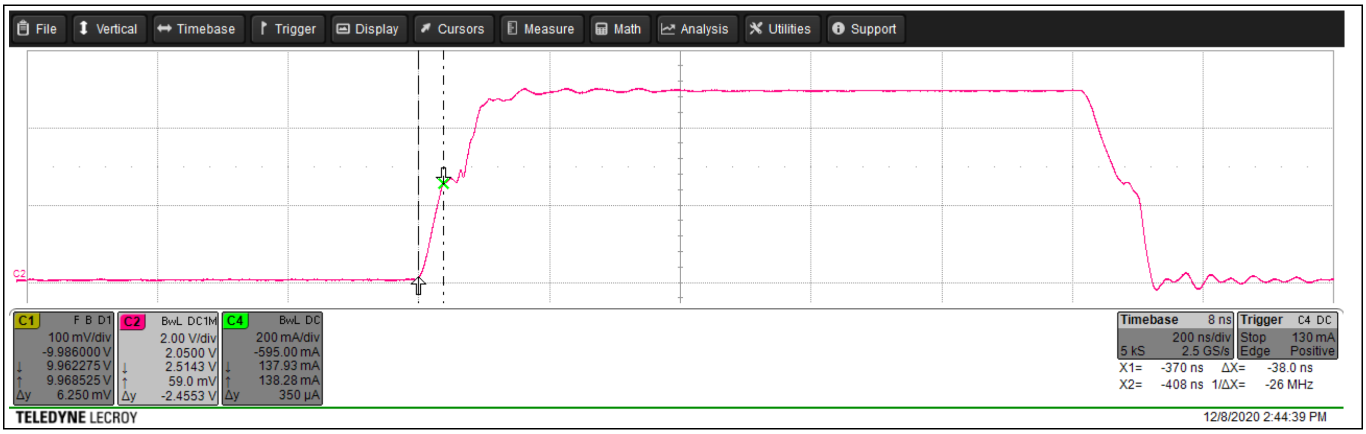

Figure 5 **V_{BSTG} with MOSFET BSS606N**

2 Buck efficiency in stop mode

During the low power mode of the application the SBC is usually used in stop mode. To decrease power consumption the buck converter uses Pulse Frequency Modulation (PFM). Figure 6 and Figure 7 show the current consumed by the SBC itself and therefore the efficiency when the application only needs few µA on VCC1.

IVS is the current on the VS pin into the SBC.
Iq is the current consumed by the SBC, which is calculated from input power and output power.

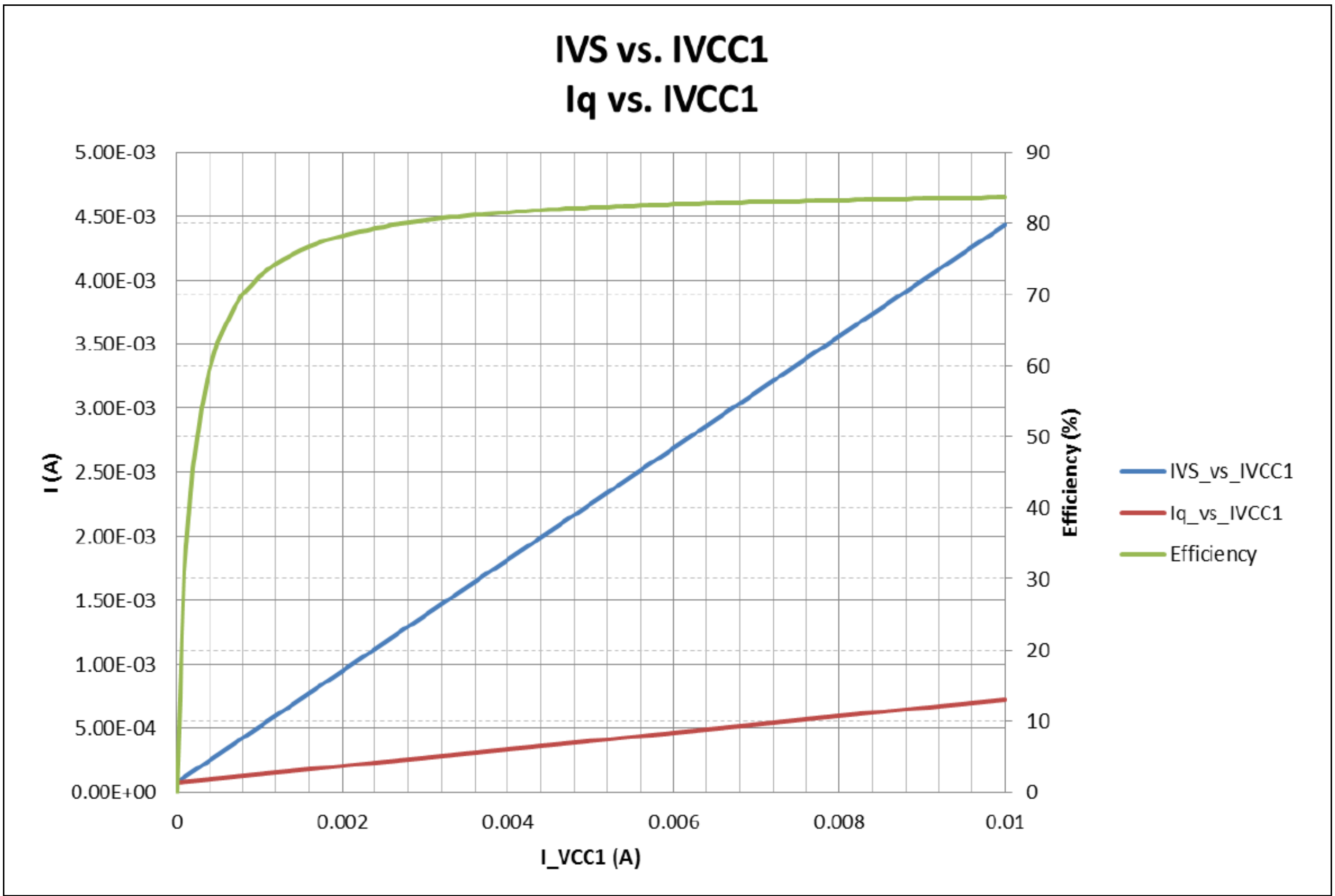

Figure 6 **Efficiency in SBC stop mode with watchdog active**

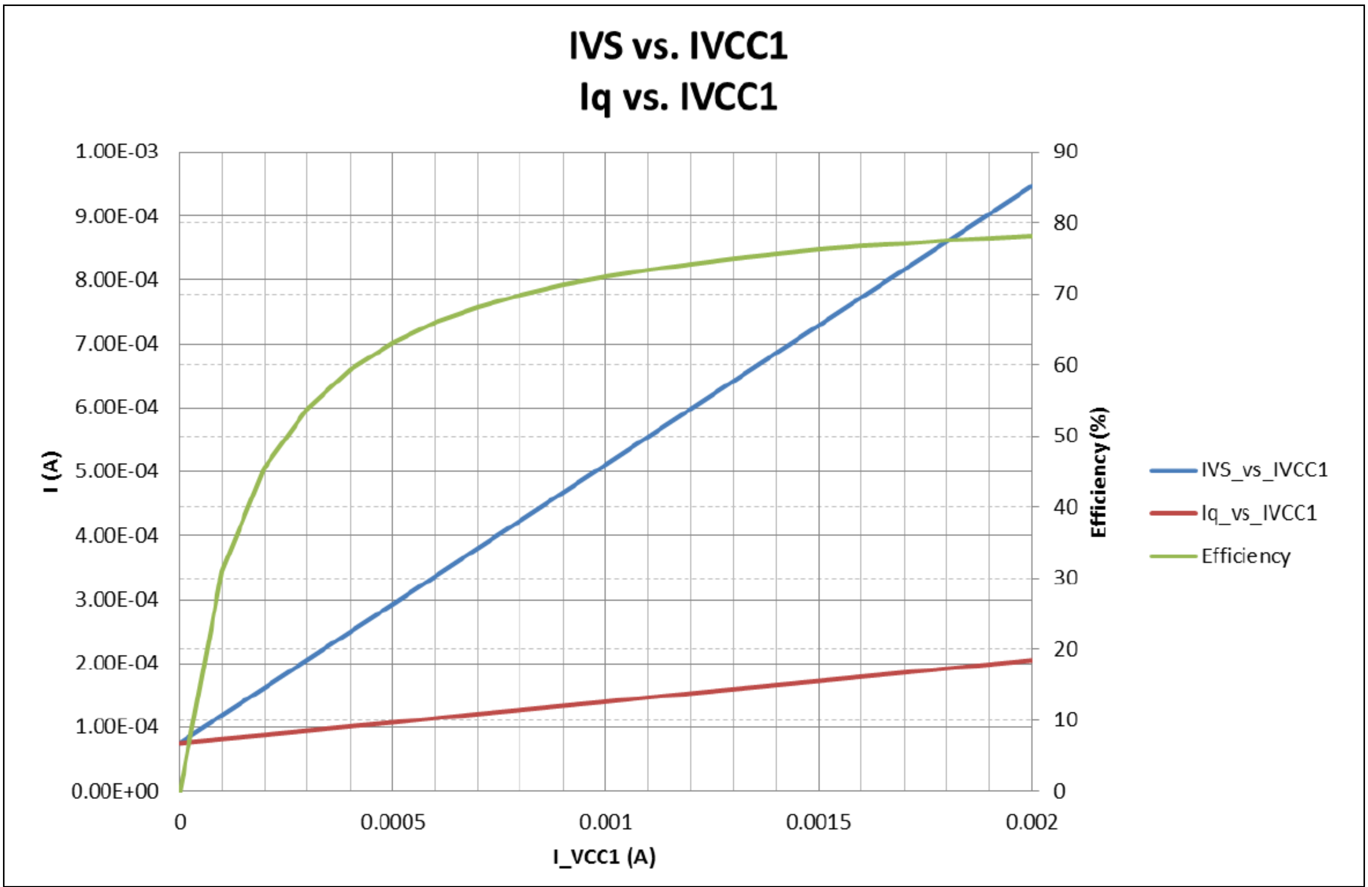

Figure 7 **Efficiency in SBC stop mode with watchdog active (Zoom in)**

The given graphs show the values for the SBC operating in stop mode with watchdog active. In case stop mode is used with disabled watchdog, the incremental current consumption adder of the watchdog can be subtracted. Which is the subtraction of P_4.4.5 – P_4.4.2 = ~15µA.

3 Recommended ground concept

Figure 8 shows the recommended PCB ground concept.

The green GND represents the board ground or the ground layer potential.

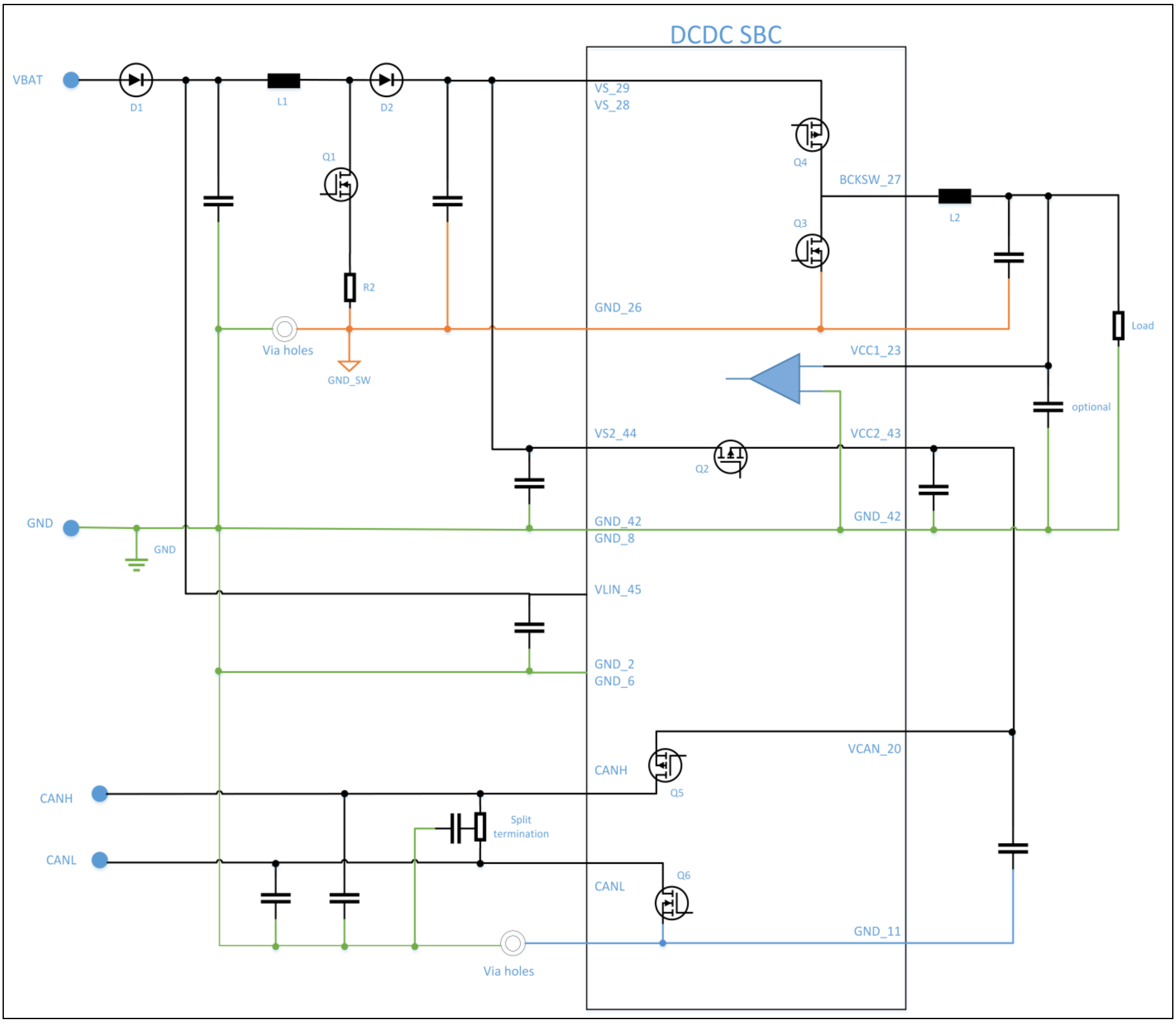

Figure 8 Recommended ground concept

Revision history

Document version	Date of release	Description of changes
1.1	2022-05-12	Initial release

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